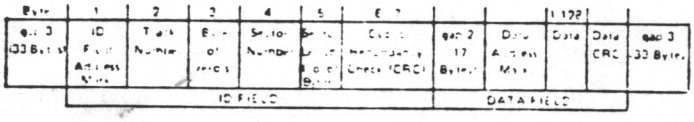
MARCH, 1978

FLOPPY DISK CONTROLLER APPLICATION NOTE

Introduction

The FD1771 is a MOS/LSI device that performs the function of interfacing a processor to a flexible (Floppy) diskette drive. This single chip replaces nearly 80% of the required disk drive interface electronics. (See figure 1-1). It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header as shown below:



The FD1771 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 1 0	=FE
	Clock	1 1 0 0 0 1 1 1	=C7
Data Address Mark	Data	1 1 1 1 1 0 1 1	=FB
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0	=F8
	Clock	1 1 0 0 0 1 1 1	=C7

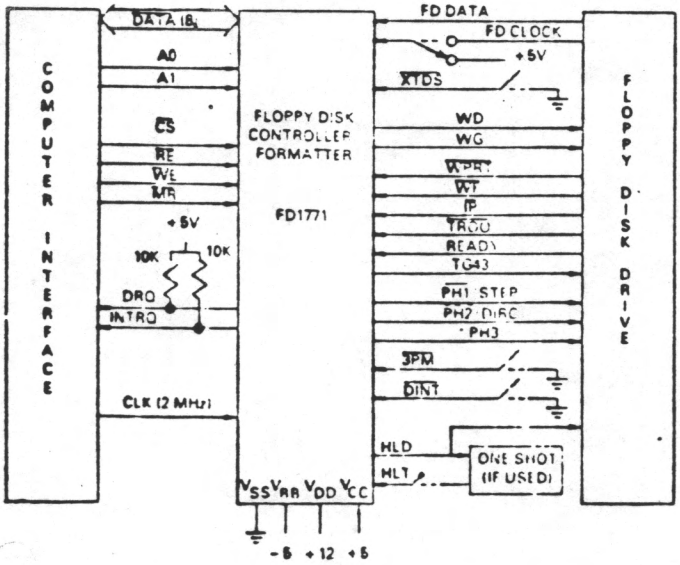
These patterns are used as synchronization codes by the FD1771 when reading data and are recorded by the formatting command, Write Track, when the FD1771 is presented with data F7 through FE.

SECTION I FD1771 DESCRIPTION

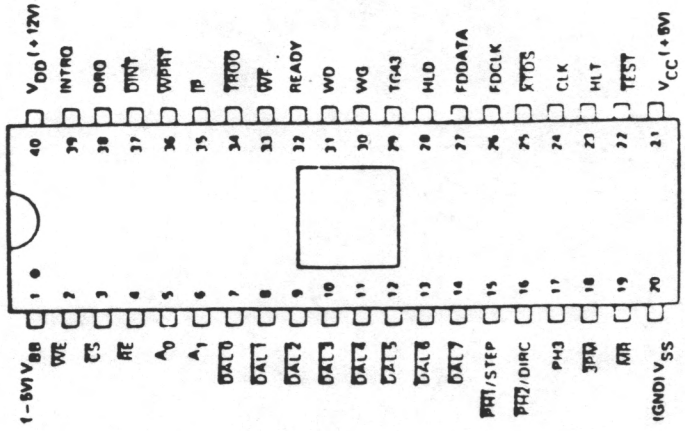
1.1 FD1771 – Flexible Drive Interface (Refer to Figure 1-1 FD1771 Block Diagram)

The FD1771 generates all controls to position the read/write head over the desired track. The FD1771 has the capability of sending successive three phase pulses over the lines PH1, PH2, and PH3 for 3 phase stepping motors or by sending a level over the PH2 line and pulses over the PH1 lines to determine direction and stepping rate for step-direction motors. The particular motor interface is chosen by hardwiring the external pin, 3PM.

ALL REFERENCE TO FD1771 DENOTES FD1771-01 VERSION



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

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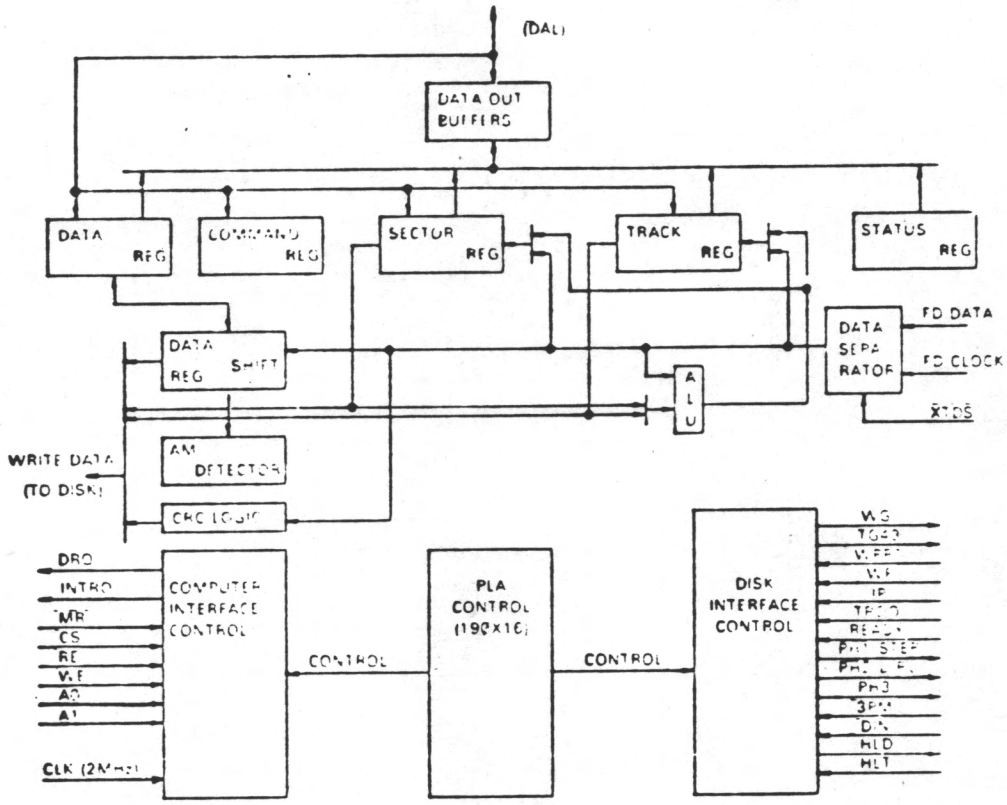

FIGURE 1-1

The head is loaded against the recording media (diskette) by the HLD (Head Load) signal from the FD1771. A read or write operation does not occur until a logic high signal is sampled at the HLT (Head Load Timing) input. This input is sampled after a 10 msec internal delay. This input may be wired high if 10 msec time is sufficient or a one shot may be used to extend this time. If the head is already engaged from a previous operation the resetting of bit 2 in the Read or Write Command (see Processor Interface) will disable the HLT functions and the 10 ms delay.

When reading the serial data from the disk the FD1771 will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and presented to the processor interface. The serial data read from the Floppy Driver may be input as composite data, both clock and data present at the FDDATA input, or as separated data in which the data is input to the FDDATA pin and the clock is input to the FD Clock

When writing, information is presented as composite of serial clock and data pulses of 500 nsec periods. With data present at the WD output the WG (Write Gate) signal is activated to allow current to flow in the Read/Write head

The remaining interface between the FD1771 and the Floppy Drive concerns status information. The IP (Index Pulse) and TROO (Track 00) signals are outputs of the drive to indicate when the index mark is encountered (once per revolution of the disk) or when the Read/Write head is located over Track 00 respectively.

The WPRT (Write Protect), DINT (Disk Initialization), and Ready signals reflect the drive condition. The Write Protect signal, when a logic low, prevents the FD1771 from executing a Write Command. The Disk Initialization input, when a logic low, prevents a Write Track Command and essentially disables the rewriting of a format over a previously formatted diskette. The Ready signal indicates Floppy Drive readiness and a logic low on this input prevents any Read or Write command from being executed.

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ther status interface signals are $\overline{WF}$ (Write Fault) from he Drive which signifies a write operation fault such as failure o detect write current when WG is turned on terminating the Current Write command; and the TG43 signal to the drive ndicating the track to be written on is located between Track 44 and Track 76. This latter signal is used by the drive to ower the write current on inner tracks and compensate for the igher density recording of these tracks.

1.2 FD1771 – Processor Interface (See figure 1-1)

All commands, status and data are transferred over the 3 state bidirectional $\overline{DAL}$ (Data Access) lines. These 8 lines pre ent an open circuit to the common processor peripheral bus until activated by the $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with $\overline{RE}$ (Read Enable) sets the $\overline{DAL}$ into the transmitter mode while the $\overline{CS}$ combined with an active WE (Write Enable) sets the $\overline{DAL}$ in the receiver mode. The information in the FD1771 resides in 5 accessible 8 bit registers. These registers are: (1) The bidirectional Data Register which acts as a parallel buffer for read or write operations, and receives the desired track number to be accessed in seek operation. (2) the Command register which receives and stores commands from ocessor, (3) The sector register which receives the de- ector number to be accessed, (4) The track register which contains the present Track position, (5) The Status Register containing information about the present operation.

The accessing of the registers is accomplished by a combination of active levels on the $\overline{CS}$, $\overline{RE}$, or $\overline{WE}$, and the register address lines A1 and A0. The Command Register can only receive information and the Status Register can only transmit information.

Two signals are available to aid in program response to the FD1771. The INTRQ (Interrupt Request) is activated by the controller whenever an operation is completed successfully or terminated by a fault. The DRQ (Data Request) signal is available as an indication of the chips readiness to transfer a byte of data during read or write operations.

A 2MHZ clock is required by the chip as a reference for all timed signals such as motor controls and data transfers. The MR (Master Reset) clears the command register and initiates a Restore (seek track 00) Command when the $\overline{MR}$ line is re- to an inactive state.

1.3 FD1771 Instructions

The FD1771 can be considered a specialized microprocessor with its own instruction repertoire. These are listed in the Tables below.

The Restore, Seek, and the three Step commands position the Read/Write head over the desired track. The Restore positions it over Track 00, the Seek poisitions it over the track specified in the Data Register, and the Step Commands position the head over an adjacent track to its present position.

The Step In moves the head inward toward the center of the disk while the Step Out moves it outward from the center. The Step Command moves the head one step in the same direction as the previous command.

The Read and Write commands are the normally executed commands when transferring information. The Read command initiates a search for a track and sector code in the ID field equal to that in the track and sector registers. When found, the data is formatted from serial to parallel and presented to the Data Register along with the setting of the DRQ signal. By setting of bit 4 in the Read (or Write) command all data records from the desired sector until the last sector on the track are sequentially assembled. The setting of bit 3 allows other combinations of byte count per sector than the standard IBM format.

The Write Command operates similar to the Read Command in multiple sector and variable sector length. All received words in the Data register are transferred to the shift register at which time the DRQ line is set. Four separate Data address marks are selectable through bits 1 and 0 which are written on the diskette prior to writing the sector data.

The Read Address command provides the next encountered ID field (6 bytes) on the diskette to the processor. This can be used to identify the track over which the head resides and can be used if one were to multiplex between two or more drives and wish to return to the first drive. This could also be accomplished by storing the track register in memory and returning it when reactivating the first drive.

The Write Track command is basically used for formatting Once the index position is located the FD1771 will request data and transfer it to the disk including all ID fields, gaps, and Data fields. Special address marks and the CRC characters are written by detecting certain data patterns. The Read track command allows the reading of the entire recorded pattern on a track including gaps. (Refer to Data Sheet for formatting details)

The final command is the Force interrupt which can be loaded into the Command register at any time. This will terminate any present operation and can also generate an interrupt under four selectable conditions.

3.4 Status Register (See Table 1, page 16)

This register contains status information associated with each of the command instructions. Bit 7 always reflects the Ready condition of the Drive while bit 0 (Busy) always defines the status of the FD1771 concerning present operations.

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
II	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

COMMAND FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)

h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track
V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

r_1r_0=00,	6ms between steps
r_1r_0=01,	6 ms between steps
r_1r_0=10,	10ms between steps
r_1r_0=11,	20ms between steps

u = Update flag (Bit 4)

u=1, Update Track register
u=0, No update

In general bit 1 reflects the state of the external DRQ signal while bit 2 indicates lost data due to overrun or underrun conditions. The Type 1 or head positioning instructions use bit 1 and 2 as a reflection of the $\overline{IP}$ and $\overline{TR00}$ inputs respectively.

Bit 3 normally indicates the encounterance of a CRC error in the ID or Data fields except for Read Track and Write Track commands in which the CRC is not checked. Bit 4 indicates that the desired track or sector was not correctly located. Bit 6 reflects the $\overline{WP}$ input on Seek and Write Commands and combines with bit 5 to identify the encountered data address mark on the Read command. Bit 5 also indicates the head engaged status on Seek commands and Write fault or Write commands.

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record
m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)
b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0=00,	FB (Data Mark)
a_1a_0=01,	FA (Data Mark)
a_1a_0=10,	F9 (Data Mark)
a_1a_0=11,	F8 (Data Mark)

TYPE III

s = Synchronize flag (Bit 0)

$\bar{s}$=0, Synchronize to AM
$\bar{s}$=1, Do not synchronize to AM

TYPE IV

I_i = Interrupt Condition flags (Bits 3-0)

I_0=1, Not Ready to Ready Transition
I_1=1, Ready to Not Ready Transition
I_2=1, Index Pulse
I_3=1, Immediate Interrupt

E=Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay
E=0, Head is assumed Engaged and there is no 10 msec Delay

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1.5 Processor Programming

Some examples of the software control of the Floppy Disk Formatter are shown in the following flow chart. The first example (Figure 1-2) shows the writing of information onto a particular track and sector. The second example (Figure 1-3) shows accessing of information from successive sectors. The third example shows how information may be sought by using Track 00 as a table of contents (Figure 1-4)

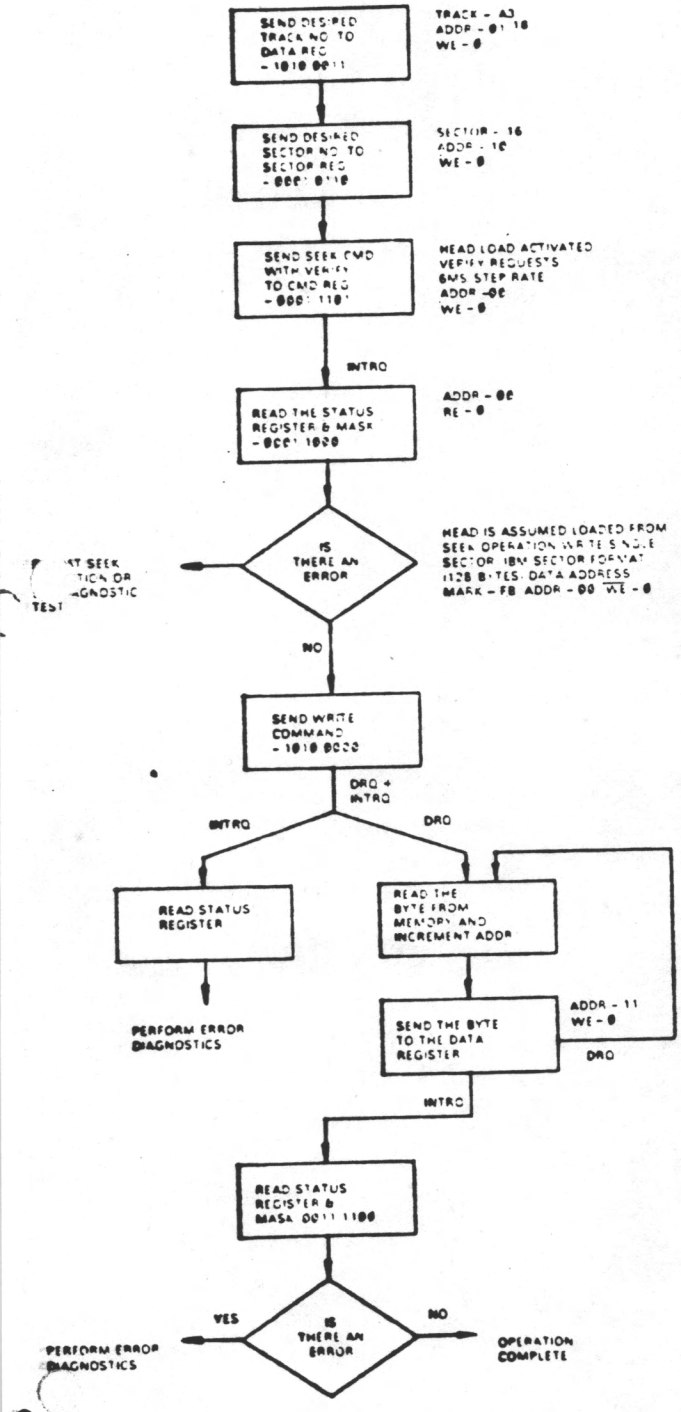

FIGURE 1-2

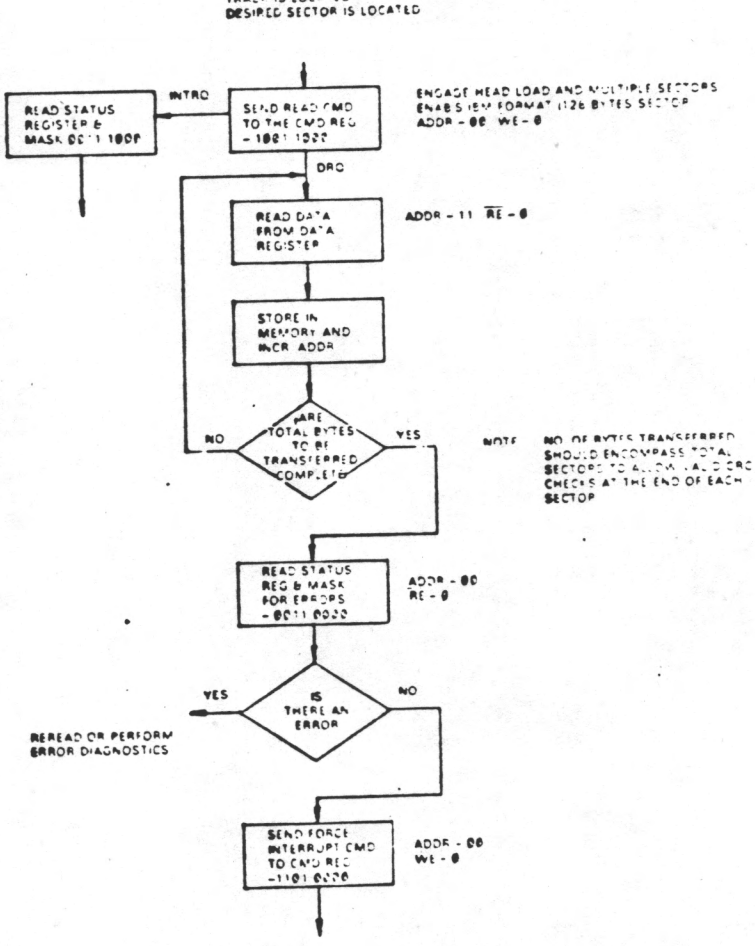

FIGURE 1-3

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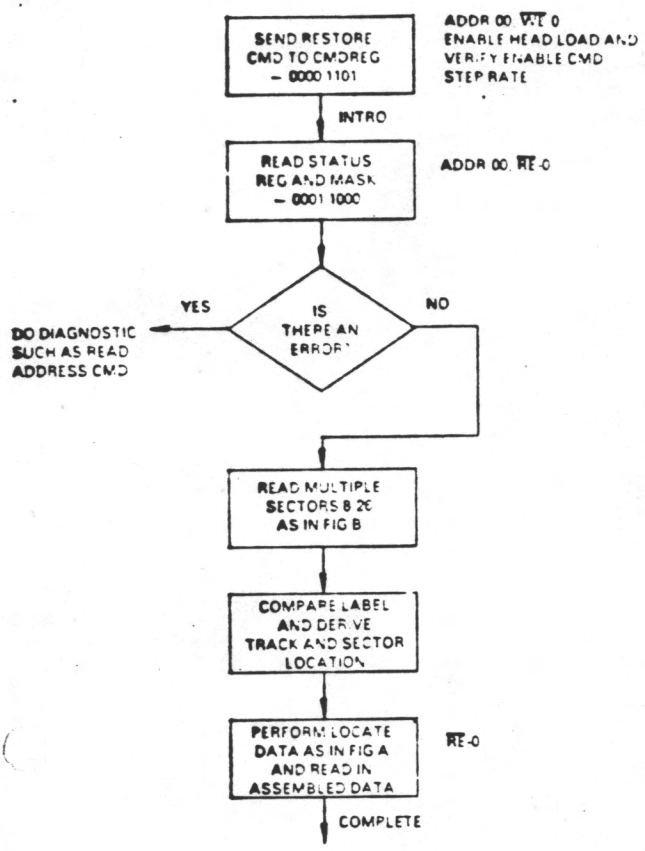

FIGURE 1-4

SECTION II FD1771 INTERFACING

2.1 System Description – Programmed Control

Figures 2-1 to 2-3 demonstrate a possible system configuration for interfacing a processor to a Floppy Disk drive utilizing the FD1771. This configuration requires the proessor to handle all data transfers which will occur as every 32 μsec.

The chip is selected by addressing it through a pre-assigned address. The lower two bits of this address selects which register is to receive or send data. The Read Enable and Write Enable strobes control the data exchange. The clock may be derived on the board or taken from other processor circuits. Generally the outputs of the FD1771 must be interfaced with drivers and receivers to provide proper matching circuits with the drive. One shots may be necessary to meet the drive's required control signal pulse widths. These circuits must be derived from recommended interfaces specified in Drive manufacturers manuals.

A clock and data separator recommended by Motorola is shown in Fugure 2-3A. This phase lock loop (PLL) circuit operates with an internal clock operating at 8MHZ or thirty two times the frequency of a received bit cell. The MC4024 is a Voltage Controlled Multivibrator that supplies the basic clock frequency. The 74LS161 counter A provides a division by 16 and supplies a carry to one side of the MC4044 phase detector. The other input to the MC4044 comes from the 74LS161 counter E carry which is affected by incoming data. The output of the phase detector is a signal proportional to the differences between the incoming pulses. This is fed through a low pass filter (for long term stability) to the input of the 4024 to control the system frequency.

The incoming raw data is shaped through a schmitt trigger and creates a pulse via flipflops G and H each time a clock or data bit is received. These pulses are stretched to 250 nsec by the one shot J and fed to nand gates. The signals are nanded with a data window or clock window and result in separated data and clock outputs.

The separator windows are formed by counter E which clocks the flip flop F at each 8 count and normally provides a 50% window every 2 μsec. Each time a bit is received it will load a count of 9 into this counter. If the system clock frequency is correct this will not alter the count. If the clock is not concurrent with information the count will be advanced or set back to alter the window and change the carry output timing.

The function of the counter D and flip flop F is to provide the proper phasing for separation of data and clock. It accomplishes this task by looking for missing clocks and data. If no clock is detected in four transitions of the OD output of counter E the output OC causes the flip flop to reverse the sampling windows.

Figures 2-3B and 2-3C illustrate two other methods of clock and data separation. The method in 2-3B incorporates a simple clock counter circuit and phasing logic. Figure 2-3C incorporates a one-shot method.

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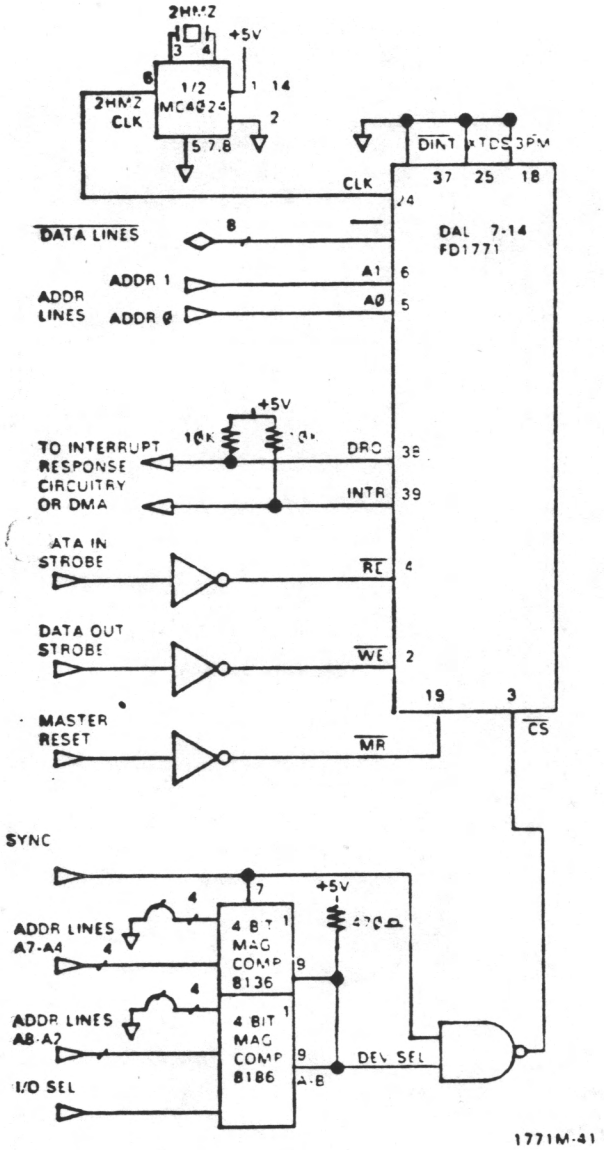

FIGURE 2-1

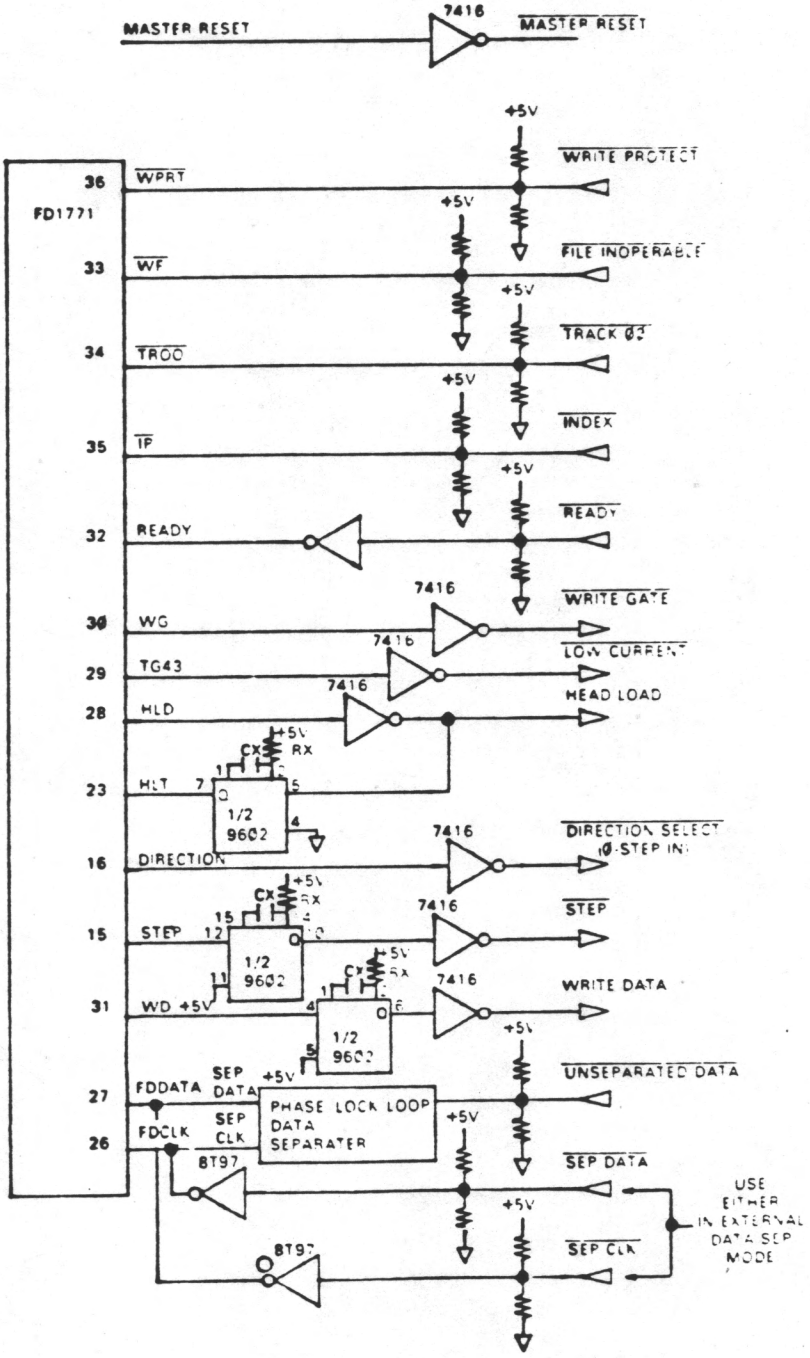

FIGURE 2-2

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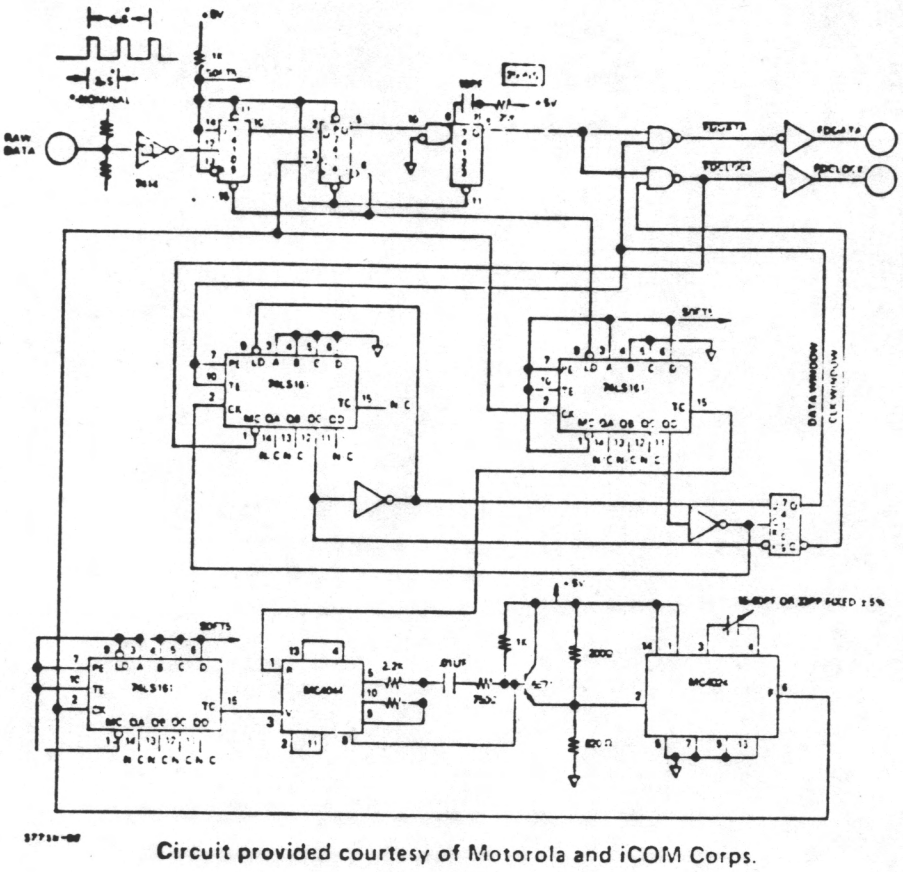
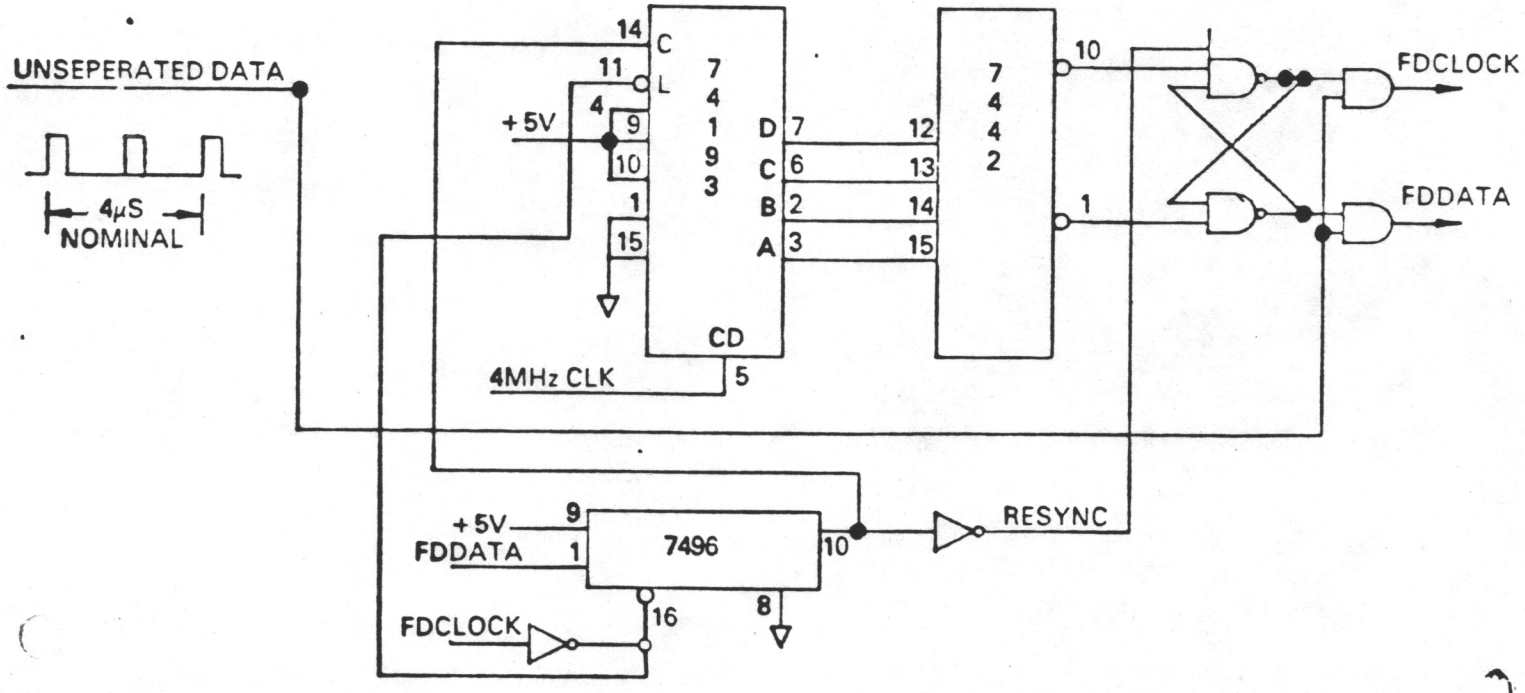


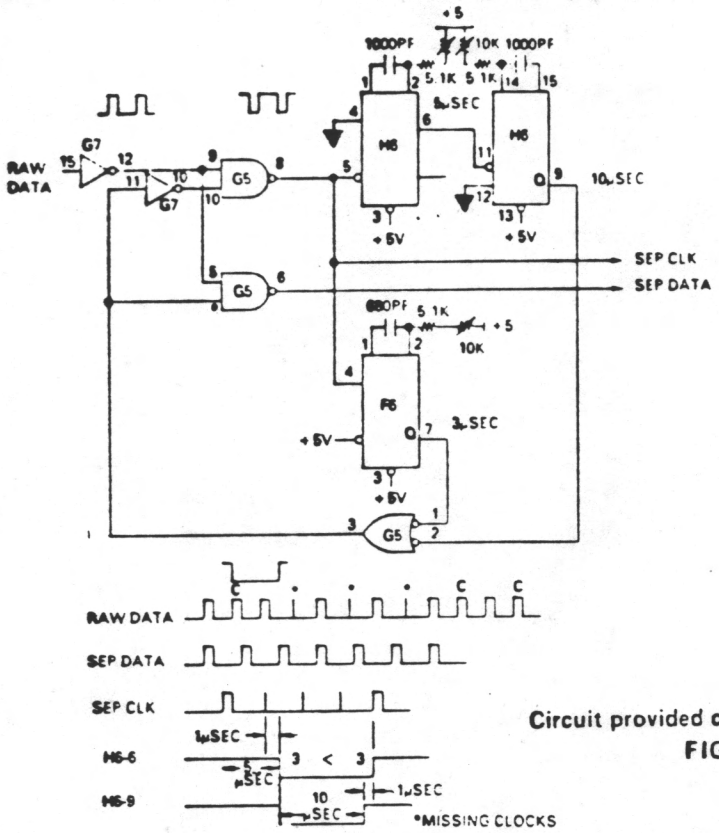
Circuit provided courtesy of Motorola and iCOM Corps.

FIGURE 2-3A



Circuit provided courtesy of Processor Applications Ltd, 2801 E. Valley View, West Covina, Ca. 91792 (213) 965-8865

FIGURE 2-3B



Circuit provided courtesy of Acutest Corp.

FIGURE 2-3C

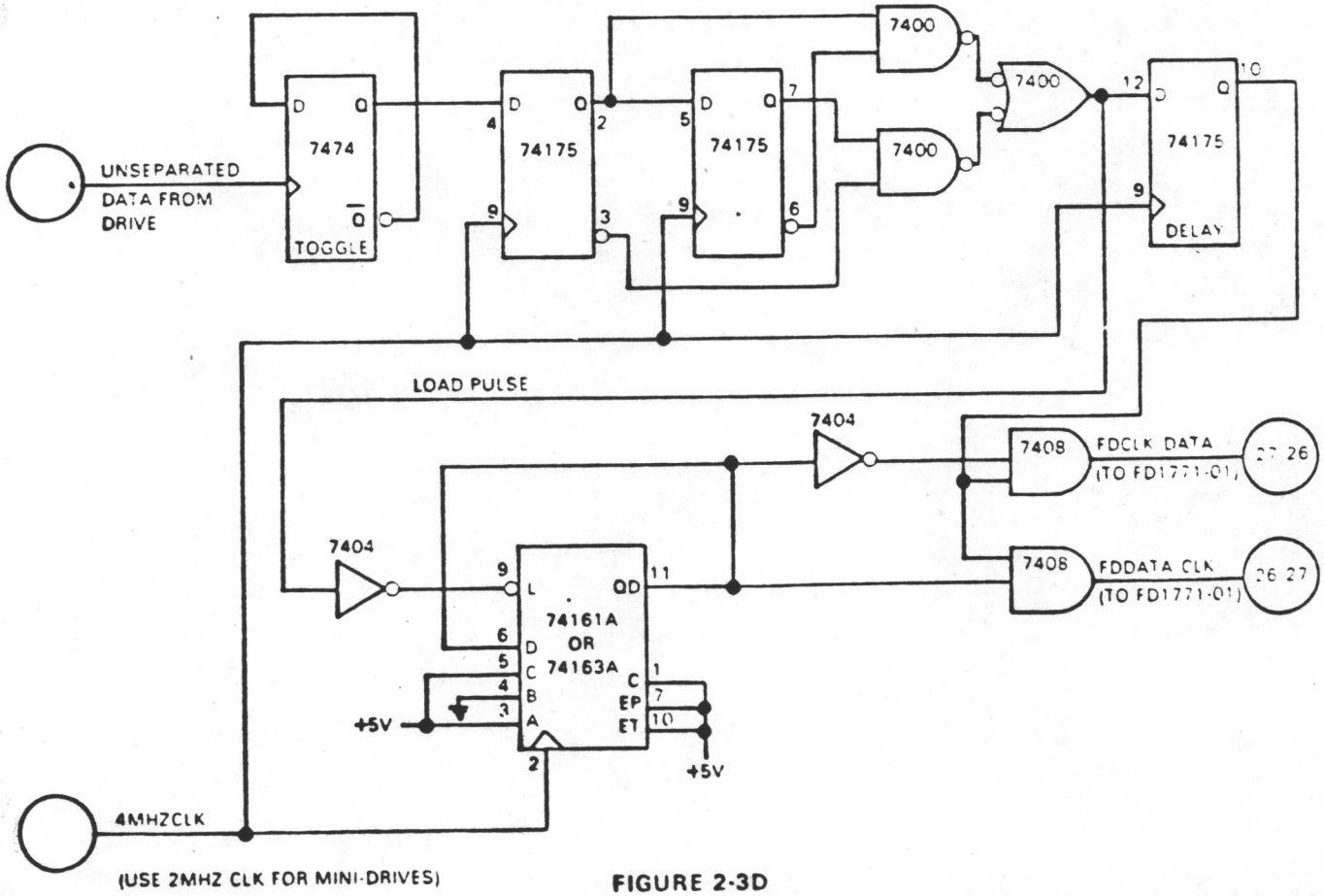


FIGURE 2-3D

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2.2 System Description – Sector buffered

In paragraph 1.1 a program controlled interface was described for the FD1771. This method uses the least number of external IC's but suffers in performance due to the necessity of the processor to service the FD1771 every 32 μsec when transferring data to or from the floppy. It may not be possible for some micro-processors to execute the program loop, within 32 μsec, therefore an alternate method of data transfer must be employed. One such method is to buffer the data transfers in a memory device, thereby requiring the processor to service only interrupt requests.

The block diagram in Figure 2-4 shows the FD1771 interface a FIFO buffer. The buffer consists of 4 FR1502 devices which provide 40 characters by 9 bits each for a total buffer storage of 160 bytes. The select logic provides proper data and command steering for block transfers or program control. The select logic will allow the processor to set a load FIFO mode, transfer a sector of information into the FIFO at processor speed, set the FIFO dump mode and send a write command to the FD1771. The data is then transferred at the rate required by the FD1771. Figure 2-5 shows the interface control and timing in the FIFO to FD interface.

When the floppy disk is to be read the processor sets the load FIFO mode and sends a Read command to the FD1771. The FD1771 then transfers data to the FIFO and interrupts the processor when a sector of information has been loaded into the FIFO. The processor will respond to the interrupt by setting the FIFO to the dump mode and then may read the data from the FIFO at processing speeds. Figure 2-6 shows the logic and timing for the FD1771 to FIFO interface.

Figure 2-7 shows the detailed logic for generating the proper control signals to the FIFO and FD1771. Figure 2-8 shows the proper connection for the FR1502 FIFO buffer memory.

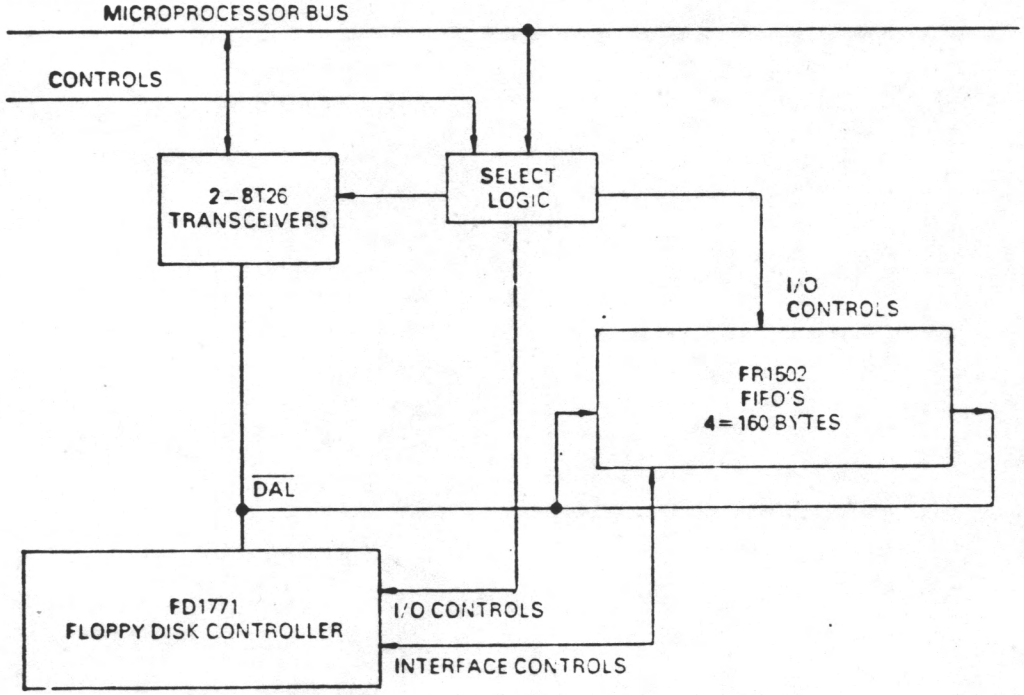
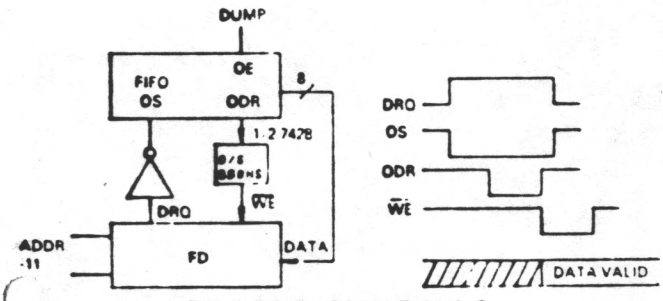
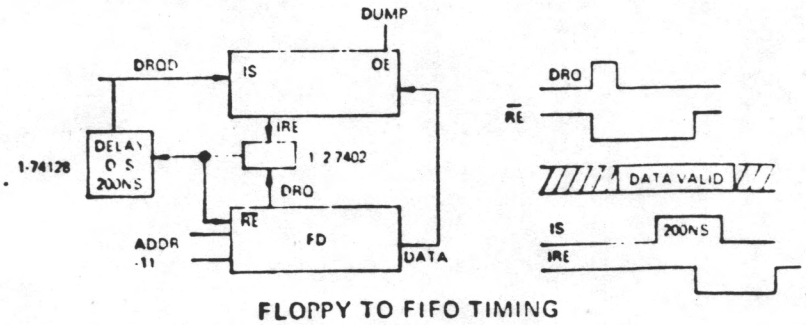


FIGURE 2-4
SECTOR BUFFER BLOCK DIAGRAM



FIFO TO FLOPPY TIMING
FIGURE 2-5



FLOPPY TO FIFO TIMING
FIGURE 2-6

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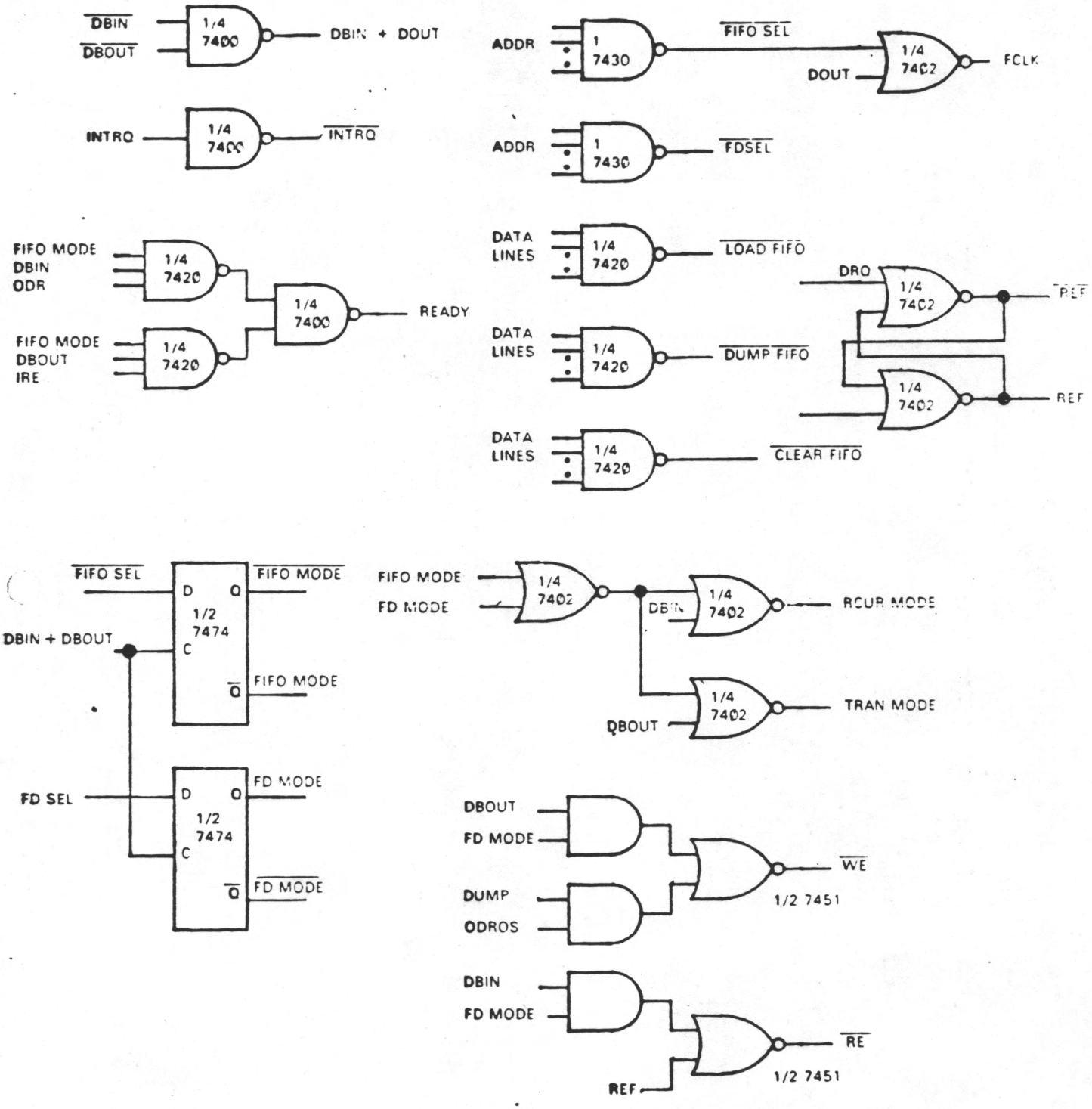

FIGURE 2-7
TIMING CONTROL

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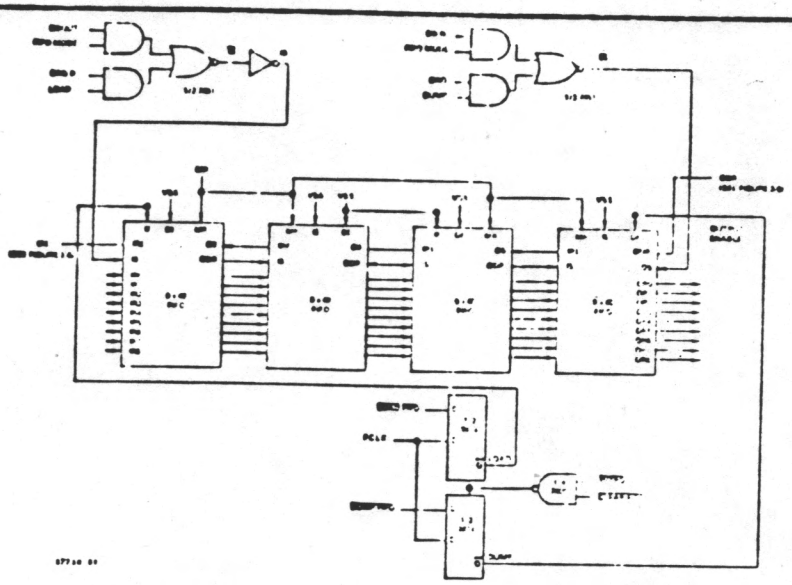

The format of the Status Register is shown below:

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table below.

YOUR LOCAL WDC REPRESENTATIVE IS.

STATUS REGISTER SUMMARY						
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE.	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to Any Input with Respect to V_{BB}	+20 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{BE} = -5.0 ± .5V,
V_{SS} = 0V, V_{CC} = +5V ± .25V
V_{DD} - 10ma Nominal, V_{CC} = 30 ma Nominal,
V_{BB} = 0.4 ua Nominal

* For complete electrical specifications see FD1771 Data Sheet.

All diagrams within this application note are shown for illustrative purposes & may not necessarily reflect the total logic to implement interface method.

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